DETAILED ACTION

The Examiner would like to thank the Applicant for the well-presented response, which was useful in the examination. The Examiner appreciates the effort to perform a careful analysis and make appropriate amendments to the claims.

Claims 1-2 and 5-30 are pending. Claims 1-2 and 5-30 have been examined. Claims 1-2 and 5-30 have been rejected.

Response to Arguments

1. The Applicant's arguments regarding the objection of claim 10 for being identical to claim 9 have been considered and are persuasive. The objection has been withdrawn.

2. The Applicant's arguments with respect to claims 1-2 and 5-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-2, 5-11, 14-19, 21-27, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stellenberg et al (U.S. Patent 6,167,364) in view of the Applicant's Admitted Prior Art, hereinafter the AAPA.

3. As per claim 1, Stellenberg teaches a method comprising:

measuring first electrical characteristics of an interconnection (col. 1 lines 65-67 and col. 2 lines 1-2); and

determining a test network that emulates the interconnection, the test network having second electrical characteristics that includes determining resistive and capacitive values such that the measured first electrical characteristics of the interconnection are approximated by the resistive and capacitive values of the test network (col. 3 lines 50-65. The local interconnect including a series of load sections with C_{row} and Z_t is a test network emulating the interconnection having second electrical characteristics which is the propagation delay of the RC models of interconnections), wherein determining the resistive and capacitive values includes adjusting the resistive and capacitive values based on the first characteristics representation (col. 7 lines 37-44. The actual measured delay data is the first characteristics representation) within a specified tolerance (the abstract, the last 4 lines).

However, Stellenberg does not teach:

generating a first graphical representation of a first output of interconnection that is based, at least in part, on the first electrical characteristics

creating a second graphical representation of a second output of the test network based on the adjusted resistive and capacitive values, wherein the second graphical representation approximates the first graphical representation of the first output of the interconnection.

The AAPA teaches generating graphical representation for electrical characteristics of electrical devices with interconnection is well known in the art (p. 6 paragraphs 0018-0019) .

It would have been obvious to one of ordinary skill in the art to combine the teachings of Stellenberg and the AAPA. The AAPA's teachings would have allowed users perform visual inspection and/or comparison of the two representations.

4. As per claim 2, Stellenberg teaches the test network is a resistive/capacitive network (col. 3 lines 50-58 and Fig. 2.)

5. As per claim 6, Stellenberg teaches the test network is a resistive network (col. 3 lines 50-58 and Fig. 2.)

6. As per claim 7, Stellenberg teaches the test network is a capacitive network (col. 3 lines 50-58 and Fig. 2.)

7. As per claim 8, Stellenberg teaches the test network is comprised of a plurality of resistive/capacitive networks (col. 3 lines 50-58 and Fig. 2.).

8. As per claim 9, Stellenberg teaches connecting the resistive/capacitive network between a driver of a first input/output circuit and a receiver of a second input/output circuit (col. 3 lines 15-22).

9. As per claim 10, these limitations have already been discussed in claim 9. They are, therefore, rejected for the same reasons.

10. As per claim 11, variable resistors and capacitors have existed for decades. It would have been obvious to one of ordinary skill in the art to use them to implement a resistive/capacitive network in order to vary their values to approximate the interconnect.

11. As per claim 14, it is well known to implement the resistive/capacitive network on a printed circuit board. It would have been obvious to one of ordinary skill in the art to implement the resistive/capacitive network on a printed circuit board, for it is economical to do so.

12. As per claim 15, Stellenberg teaches an apparatus comprising:

an integrated circuit having at least one input/output ports, the at least one input/output ports having a driver and a receiver (col. 3 lines 15-19).

a test network having second electrical characteristics that include resistive and capacitive values, the test network electrically coupling the driver and the receiver such that the input/output interface interconnection (col. 3 lines 50-65. The local interconnect including a series of load sections with C_{row} and Z_t is a test network emulating the interconnection having second electrical characteristics which is the propagation delay of the RC models of interconnections) having first electrical characteristics is emulated therewith, wherein the

resistive and capacitive values are adjusted based on a first graphical representation of a first output of the input/output interface interconnection that is generated based, at least in part, on the first electrical characteristics (col. 7 lines 37-44).

However, Stellenberg does not teach first graphical representation not generating a second graphical representation.

The AAPA teaches The AAPA teaches generating graphical representation for electrical characteristics of electrical devices with interconnection is well known in the art (p. 6 paragraphs 0018-0019).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Stellenberg and the AAPA. The AAPA's teachings would have allowed users perform visual inspection and/or comparison of the two representations.

13. As per claim 16, these limitations have already been discussed in claim 2. They are, therefore, rejected for the same reasons.

14. As per claim 17, these limitations have already been discussed in claim 6. They are, therefore, rejected for the same reasons.

15. As per claim 18, these limitations have already been discussed in claim 7. They are, therefore, rejected for the same reasons.

16. As per claim 19, these limitations have already been discussed in claim 11. They are, therefore, rejected for the same reasons.

17. As per claim 21, these limitations have already been discussed in claim 14. They are, therefore, rejected for the same reasons.

18. As per claim 22, the AAPA teaches IO circuit interface on an IC, which is a part of a microprocessor (p. 3 paragraph 0007).

19. As per claim 23, these limitations have already been discussed in claim 1. They are, therefore, rejected for the same reasons.

20. As per claim 24, these limitations have already been discussed in claim 2. They are, therefore, rejected for the same reasons.

21. As per claim 25, these limitations have already been discussed in claim 1. They are, therefore, rejected for the same reasons.

22. As per claim 26, these limitations have already been discussed in claim 8. They are, therefore, rejected for the same reasons.

23. As per claim 27, these limitations have already been discussed in claim 8. They are, therefore, rejected for the same reasons.

24. As per claim 29, these limitations have already been discussed in claim 1. They are, therefore, rejected for the same reasons.

25. As per claim 30, these limitations have already been discussed in claim 1. They are, therefore, rejected for the same reasons.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stellenberg in view of the AAPA as applied to claims 16 above, and further in view of Ward (U.S. Pat. 5,456,241).

26. As per claim 5, Stellenberg does not teach the tolerance of 10%.

However, Ward teaches this limitation (col. 6 lines 56-58).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Stellenberg, the AAPA, and Ward. Ward's teachings would have allowed the tolerance to meet the conventional agreement (col. 6 lines 56-58).

Claims 12-13, 20, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stellenberg in view of the AAPA as applied to claims 11 and 27 above, and further in view of Neil et al (Principles of CMOS VLSI DESIGN A System Perspective, 2nd Edition, Addison-Wesley Publishing Company, 1993).

27. As per claim 12, Stellenberg does not teach the resistive/capacitive network is implemented on an integrated circuit chip.

However, Neil teaches implementing resistors and capacitors on an integrated circuit (pp. 134-135, section 3.3.2).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Stellenberg, the AAPA, and Neil. Neil's teachings would have provided high-quality

capacitor and resistors of variable characteristics (p. 130 section 3.3 1st paragraph of this section).

28. As per claim 13, it is well known to one of ordinary skill in the art a capacitor is can be implemented with gate capacitance. Therefore, it would have been obvious to one of ordinary skill in the art to use distributed gate capacitance to implement the capacitance.

29. As per claim 20, these limitations have already been discussed in claim 12. They are, therefore, rejected for the same reasons.

30. As per claim 28, these limitations have already been discussed in claim 12. They are, therefore, rejected for the same reasons.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong V. Luu whose telephone number is 571-272-8572. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah, can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Cuong V Luu/

Examiner, Art Unit 2128

/Kamini S Shah/

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